**WHAT IS CLAIMED IS:**

1. A liquid crystal display comprising:

a plurality of first wires which transmits first signals, extend in a direction, and are substantially parallel to each other;

a plurality of second wires which transmits second signals and substantially parallel to the first wires;

a first shorting bar which is connected to the first wires;

a second shorting bar which is connected to the second wires; and

a main shorting bar which is located outside the first and the second wires.

2. A liquid crystal display of claim 1 wherein the first and the second wires are gate lines, and the first and the second signals are scanning signals.

3. A liquid crystal display of claim 1 wherein the first and the second wires are data lines, and the first and the second signals are image signals.

4. A liquid crystal display of claim 1 wherein the main shorting bar is connected to the first and the second wires.

5. A liquid crystal display of claim 1 wherein the first and the second wires are alternately arranged one after another.

6. A liquid crystal display comprising:

an insulating substrate;

a plurality of gate lines which are formed on the substrate in the horizontaldirection;

a gate insulating film which covers the gate lines and has first contact holes exposing portions of the gate lines;

a plurality of data lines which are formed on the gate insulating film, extend in a vertical direction, and intersect the gate lines;

a first shorting bar which is formed on the gate insulating film and extends in the vertical direction;

a second shorting bar which is formed on the gate insulating film and substantially parallel to the first shorting bar;

a passivation film which covers the data line and the first and the second shorting bars, and has second contact holes on the first contact holes and third and fourth contact holes respectively over the first and the second shorting bars;

a first connecting member which is formed on the passivation film and connected to a first group of the gate lines through the first and the second contact holes and to the first shorting bar through the third contact hole; and

a second connecting member which is formed on the passivation film and connected to a second group of the gate lines which are not connected to the first connecting member through the first and the second contact holes and to the second shorting bar through the fourth contact hole.

7. A liquid crystal display of claim 6, further comprising:

a third, a fourth and a fifth shorting bars which is formed on the substrate and extend in the horizontal direction;

a third, a fourth and a fifth connecting members formed on the passivation film,

wherein the third, the fourth and the fifth connecting members respectively connect the data lines to the third, the fourth and the fifth shorting bars.

8. A liquid crystal display of claim 7, wherein the passivation film has fifth contact holes exposing the data lines, and the passivation film and the gate insulating film has sixth, seventh and the eighth contact holes respectively exposing the third, the fourth and the fifth shorting bars, wherein the third, the fourth and the fifth connecting members are respectively connected to the data lines through the fifth contact holes, and to the third, the fourth and the fifth shorting bars through the sixth, the seventh and the eighth contact holes.

9. A liquid crystal display of claim 6, further comprising a gate shorting bar which is formed on the substrate and connected to the gate lines.

10. A liquid crystal display of claim 9, further comprising a data shorting bar which is formed on the gate insulating film and connected to the data lines.

11. A liquid crystal display of claim 10, wherein the data shorting bar is electrically connected to the gate shorting bar.

12. A liquid crystal display of claim 6, further comprising a gate shorting bar which is formed on the substrate, extends in the vertical direction,

and is located opposite the gate lines with respect to the first and the second shorting bars and separated from the gate lines.

13. A liquid crystal display of claim 12, further comprising a data shorting bar which is formed on the gate insulating film, extends in the horizontal direction, and is located opposite the data lines with respect to the third, the fourth and the fifth shorting bars and separated from the data lines.

14. A liquid crystal display of claim 13, wherein the data shorting bar is electrically connected to the gate shorting bar.

15. A liquid crystal display comprising:

an insulating substrate;

a plurality of gate lines which are formed on the substrate and extend in a horizontal direction;

a first shorting bar which is formed on the substrate and extends in the horizontal direction;

a second shorting bar which is formed on the substrate and substantially parallel to the first shorting bar;

a gate insulating film which covers the gate lines and the first and the second shorting bars, and has first and a second contact holes exposing the first and the second shorting bars;

a plurality of data lines which are formed on the gate insulating film, extend in the vertical direction, and intersect the gate lines;

a passivation film which covers the data lines and the first and the second shorting bars, and has a third and a fourth contact holes on the first and

the second contact holes and fifth contact holes over the data lines;

a first connecting member which is formed on the passivation film and connected to a first group of the data line through the first and the third contact holes and to the first shorting bar through the fifth contact hole; and

a second connecting member which is formed on the passivation film and connected to a second group of the data lines which are not connected to the first connecting member through the second and the fourth contact holes, and to the second shorting bar through the fifth contact hole.

16. A liquid crystal display of claim 15, further comprising a gate shorting bar which is formed on the substrate and connected to the gate lines.

17. A liquid crystal display of claim 16, further comprising a date shorting bar which is formed on the gate insulating film and connected to the data lines.

18. A liquid crystal display of claim 17, wherein the data shorting bar is electrically connected to the gate shorting bar.

19. A liquid crystal display of claim 15, further comprising a data shorting bar which is formed on the gate insulating film, extends in the horizontal direction, is located opposite the data lines with respect to the first and the second shorting bars and separated from the data lines.

20. A liquid crystal display of claim 19, further comprising a gate shorting bar which is formed on the substrate, extends in the vertical direction and is separated from the gate lines.

21. A liquid crystal display of claim 20, wherein the gate shorting bar is electrically connected to the data shorting bar.

22. A manufacturing method of a liquid crystal display comprising the steps of:

depositing a metal layer;

patterning the metal layer to form gate lines;

forming a gate insulating film which covers the gate lines;

forming data lines and a first and a second shorting bars for testing the gate lines on the gate insulating film;

depositing a passivation film;

etching the passivation film and the gate insulating film to form first, a second and a third contact holes respectively exposing the gate lines and the first and the second shorting bars;

depositing a conductive layer; and

patterning the conductive layer to form a pixel electrode, a first connecting member which is connected to the gate lines and the first shorting bar through the first and the second contact holes, and a second connecting member which is connected to the gate line and the second shorting bar through the first and the third contact holes.

23. A manufacturing method of a liquid crystal display according to claim 22, further comprising the step of forming a third shorting bar for electrostatic discharge protection which is connect d to the gate lines by patterning the metal layer.

24. A manufacturing method of a liquid crystal display according to claim 23, further comprising the step of disconnecting the third shorting bar from the gate lines after forming the first and the second connecting members.

25. A manufacturing method of a liquid crystal display comprising the steps of:

forming gate lines, a first, a second and a third shorting bars for testing data lines on a substrate;

forming a gate insulating film;

depositing a metal layer on the gate insulating film;

patterning the metal layer to form data lines;

depositing a passivation film;

etching the passivation film and the gate insulating film to form first, second, third and fourth contact holes exposing the data line, the first, the second and the third shorting bars;

depositing a conductive layer; and

patterning the conductive layer to form a pixel electrode and connecting members which are connected to the data lines through the first contact holes and to the first, the second and the third shorting bars through the second, the third and the fourth contact holes.

26. A manufacturing method of a liquid crystal display of claim 25, further comprising the step of forming a fourth shorting bar for electrostatic discharge protection which is connected to the data lines by patterning the metal layer.

27. A manufacturing method of a liquid crystal display of claim 26, further comprising the step of disconnecting the fourth shorting bar from the data lines after forming the first, the second and the third connecting members.

28. A manufacturing method of a liquid crystal display comprising the steps of:

forming a wire including a plurality of gate lines, a plurality of data lines; a main shorting bar for electrostatic discharge protection which is connected to the gate lines and the data lines, a first and a second shorting bars for testing the gate lines, a third and a fourth shorting bars for testing the data lines, wherein the first and the second shorting bars are alternately connected to the gate lines and the third and the fourth shorting bars are respectively connected to the every other data lines;

separating the main shorting bar from the gate and the data lines; and

applying voltages to the first, the second, the third and the fourth shorting bars for detecting defects of the data lines and the gate lines.

29. A manufacturing method of a liquid crystal display of claim 28, wherein the voltages applied to the first shorting bar and the second shorting bar are different.

30. A manufacturing method of a liquid crystal display of claim 28, wherein the voltages applied to the third shorting bar and the fourth shorting bar are different.

31. A manufacturing method of a liquid crystal display of claim 28, further comprising the step of removing the first, the second, the third and the

fourth shorting bars after the step of applying voltages.

32. A testing method of a liquid crystal display having a plurality of pixels arranged in a matrix shape, a plurality of first gate lines connected to the pixels in odd rows, a plurality of second gate lines connected to the pixels in even rows, and a plurality of first, second and third data lines which are connected to the pixels in different columns and arranged in three shifts, comprises the steps of:

applying a first pulse to the first gate lines at a first time;

applying a second pulse to the second gate lines at a second time;

applying a first and a second signals having the same polarity to the first and the second data lines, and a third signal having polarity opposite the first and the second signals to the third data lines at the first time; and

applying the first and the second signals to the second and the third data lines, and the third signal to the first data lines at the second time.

33. A testing method of claim 32, wherein the first and the second pluses are applied in periods and one of the first and the second times follows the other by a half frame.

34. A testing method of claim 32, further comprising the steps of:

applying a third pulse to the first gate lines at a third time;

applying a fourth pulse to the second gate lines at a fourth time;

applying the first and the second signals to the second and the third data lines and the third signal to the first data lines at the third time; and

applying the first and the second signals to the first and the third data lines and the third signal to the second data lines at the fourth time.

35. A testing method of the claim 34, wherein the third and the fourth pulses are applied in periods and one of the third and the fourth times follows the other by a half frame.

36. A testing method of a liquid crystal display having a plurality of pixels arranged in a matrix shape, a plurality of first gate lines connected to the pixels in odd row, a plurality of second gate lines connected to the pixels in even rows, and a plurality of first, second and third data lines which are connected to the pixels in different columns and arranged in three shifts, comprising the steps of:

applying a first pulse to the first gate lines at a first time;

applying a second pulse to the second gate lines at a second time;

applying a first signal having a polarity inverting in a first inversion period to the first and the second data lines, and a second signal having polarity opposite the first signal to the third data lines at the first time; and

applying the second signal to the first and the second data lines, and the first signal to the third data lines at the second time.

37. A testing method according to claim 36, further comprising the steps of:

applying a third pulse to the first gate lines at a third time;

applying a fourth pulse to the second gate lines at a second time;

applying the first signals to the first and the third data lines and the second signal to the second gate data lines at the third time; and

applying the first signal to the second data line and the second signal to the first and the third data lines at the fourth time.

38. A testing method according to claim 37, wherein one of the first and the second times, or one of the third and the fourth times follows the other by a half frame.

39. A testing method according to claim 37, wherein the first, the second, the third and the fourth times are a moment when the first and the second signals are inverted.

40. A testing method according to claim 39, wherein the first inversion period is the same as the width of each of the first to the fourth pulses.

41. A testing method according to claim 39, wherein the inversion period is twice the width of each of the first to the fourth pulses.

42. A testing method according to claim 37, wherein the first to the fourth times are interposed between points of time when first and the second signals are inverted.

43. A testing method according to claim 42, wherein the first inversion period is larger than the width of each of the first to the fourth pulses.